# N- and P-Channel 30-V (D-S) MOSFET

## CHARACTERISTICS

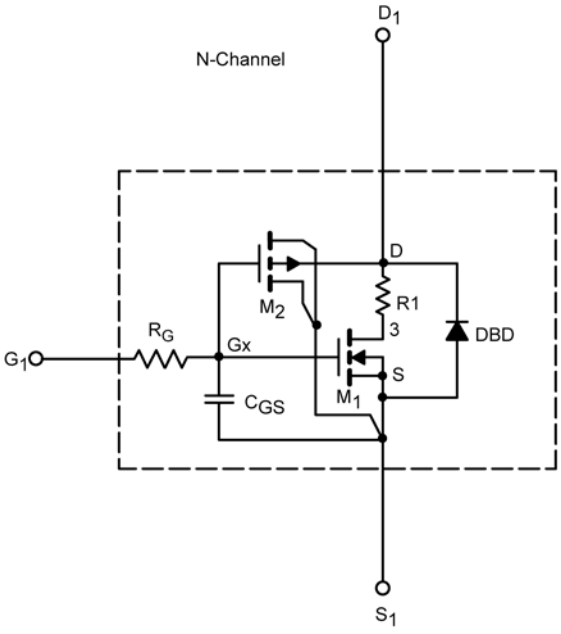
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

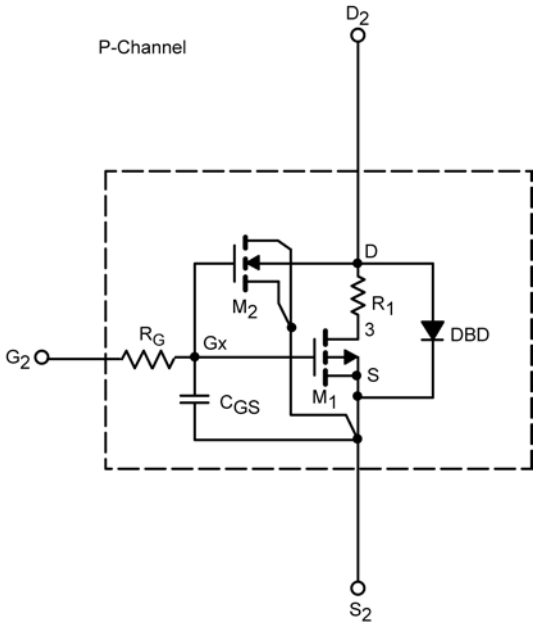
## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC



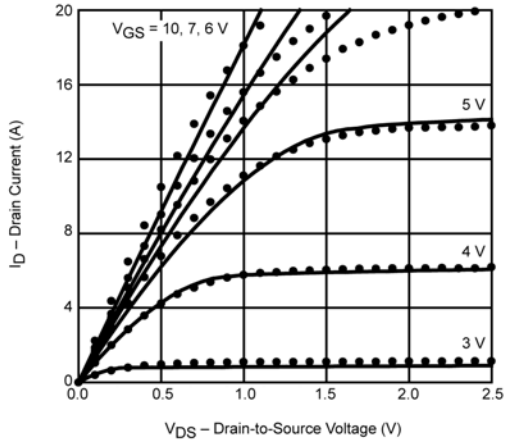

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

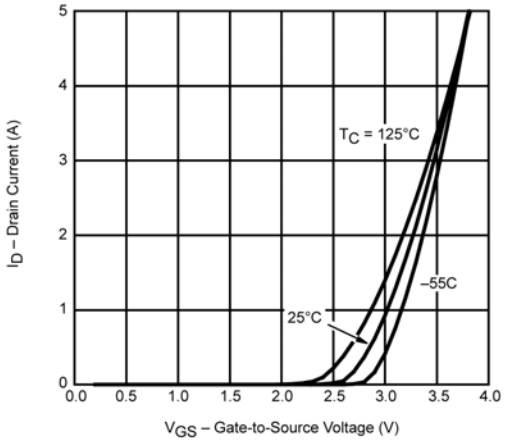
| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | N-Ch | 2 | | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | P-Ch | 2.2 | | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 10 V | N-Ch | 76 | | A |
| | | $V_{DS}$ = –5 V, $V_{GS}$ = –10 V | P-Ch | 40 | | |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 3.1 A | N-Ch | 0.054 | 0.053 | Ω |
| | | $V_{GS}$ = –10 V, $I_D$ = –2.1 A | P-Ch | 0.112 | 0.112 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 1 A | N-Ch | 0.081 | 0.081 | |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –0.43 A | P-Ch | 0.180 | 0.188 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 3.1 A | N-Ch | 5.6 | 5 | S |
| | | $V_{DS}$ = –15 V, $I_D$ = –2.1 A | P-Ch | 6.3 | 3.5 | |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 2.6 A | N-Ch | 0.78 | 0.80 | V |
| | | $I_S$ = –2 A | P-Ch | 0.80 | –0.80 | |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_D$ = 3.6 A | N-Ch | 3.4 | 4.5 | nC |
| | | $V_{DS}$ = – 15 V, $V_{GS}$ = –10 V, $I_D$ = – 2.5 A | P-Ch | 3.2 | 4.5 | |
| | | N-Channel $V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_D$ = 3.6 A P-Channel $V_{DS}$ = – 15 V, $V_{GS}$ = –4.5 V, $I_D$ = – 2.5 A | N-Ch | 1.7 | 2 | |
| | | | P-Ch | 1.8 | 2.2 | |
| Gate-Source Charge | $Q_{gs}$ | | N-Ch | 0.70 | 0.70 | |
| | | | P-Ch | 0.70 | 0.70 | |
| Gate-Source Charge | $Q_{gs}$ | | N-Ch | 0.70 | 0.70 | |
| | | | P-Ch | 1 | 1 | |

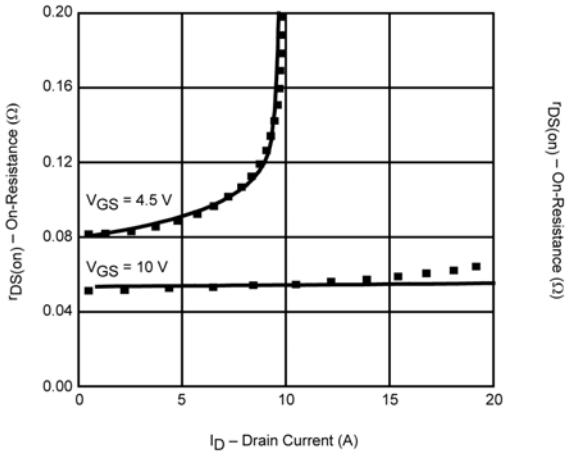
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

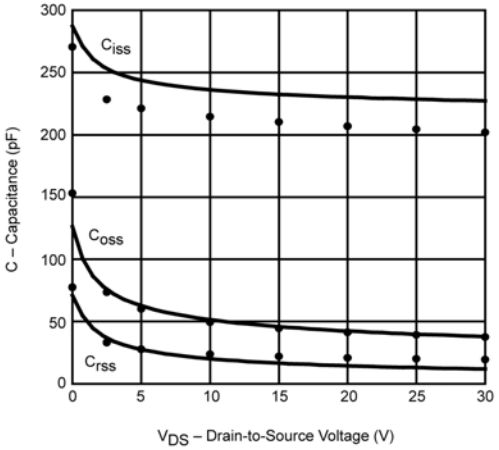
COMPARISON OF MODEL WITH MEASURED DATA ($T_J$=25°C UNLESS OTHERWISE NOTED)

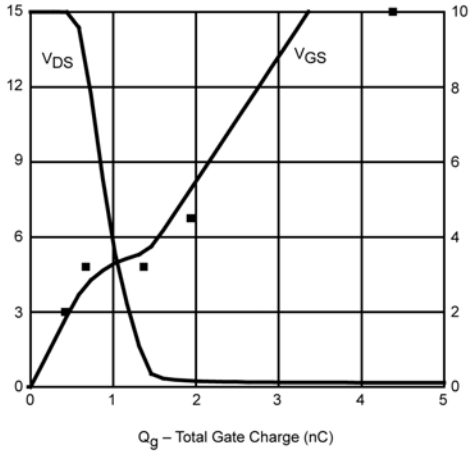
**N-Channel MOSFET**

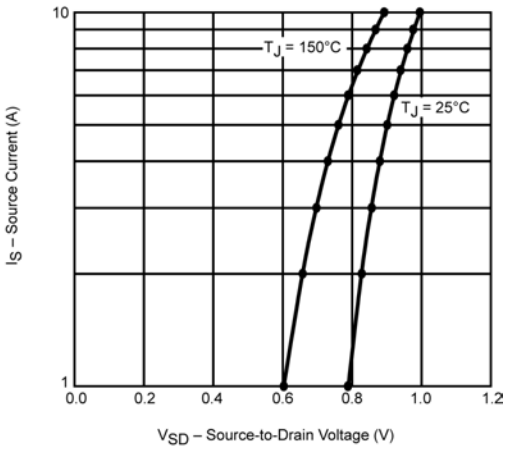


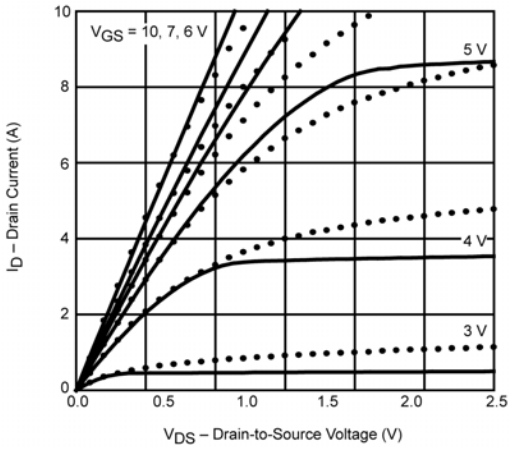



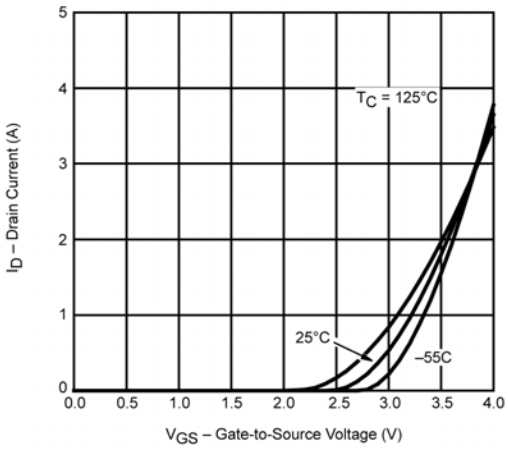



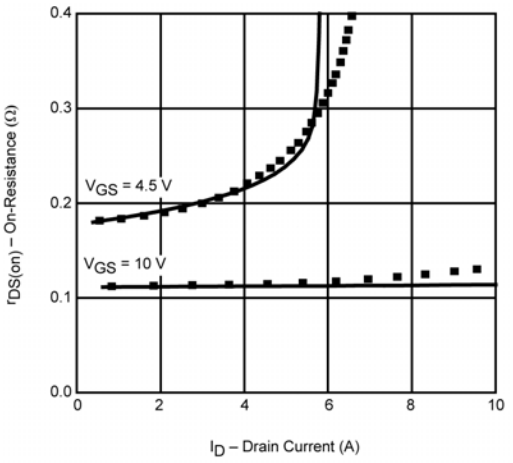



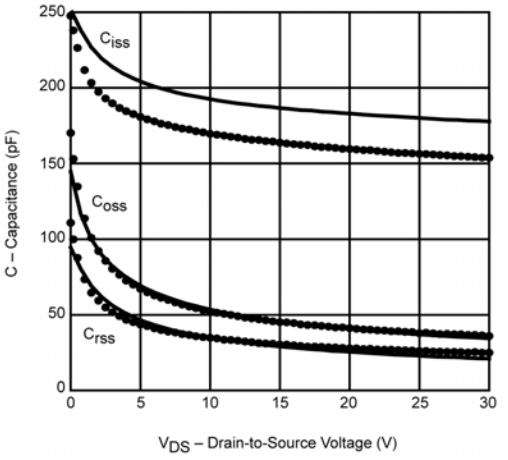

Note: Dots and squares represent measured data.

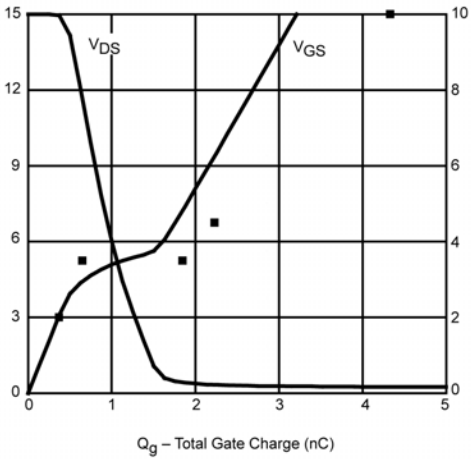
**P-Channel MOSFET**

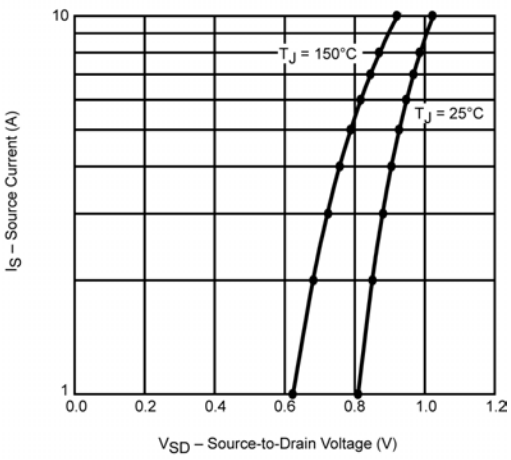



Note: Dots and squares represent measured data.

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